盛光科技股份有限公司
Most I & T Corporation

IDE Flash Disk

SI Series

Product Specification

V1.0

盛光科技股份有限公司
Most I & T Corporation

Contents:

1 Product Information

The IDE Flash Disk is solid-state design and IDE compatible. It is an ideal replacement for standard IDE hard disk. It's a solid-state design offers no seek errors even under extreme shock and vibration conditions. The IDE Flash Disk is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage, allowing simple use for the end user. The IDE Flash Disk is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. It provides memory storage for mobile computing applications, consumer electronics and embedded systems.

The IDE Flash Disk is offering various capacities. It has low power consumption and can operate from a single 3.3/5.0 Volt power supply. The operating temperature grade is standard operating temperature grade (0℃~+70℃) and wide operating temperature grade (-40℃~+85℃).

2 System Features

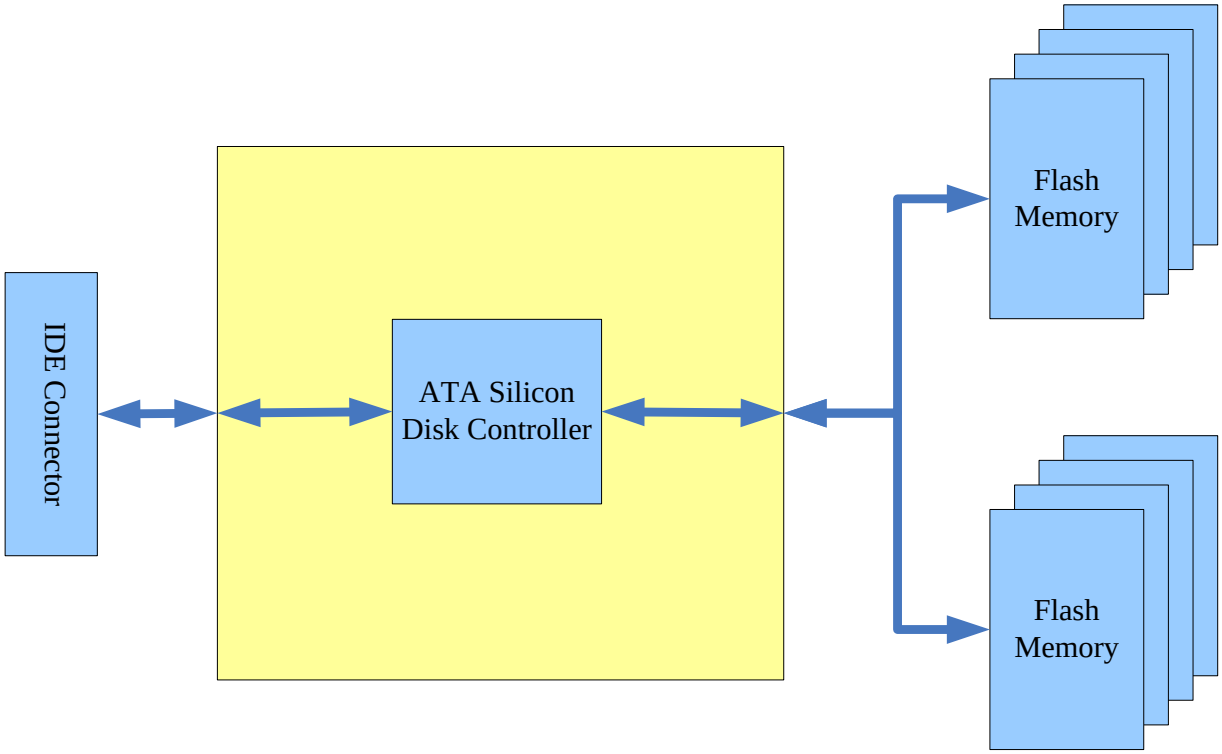
- Max Capacity supported: 64GByte.
- High reliability assured based on the internal ECC (Error Correcting Code) function.
- Reliable wear-leveling algorithm to ensure the best of flash endurance.
- Flexible file system structure.
- Automatic Recognition and Initialization of flash devices.
- Excellent performance supporting Ultra DMA Mode 4.
- Capacity supported: 128MB, 256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB, 32GB and 64GB (Unformat)

3 Product Specifications

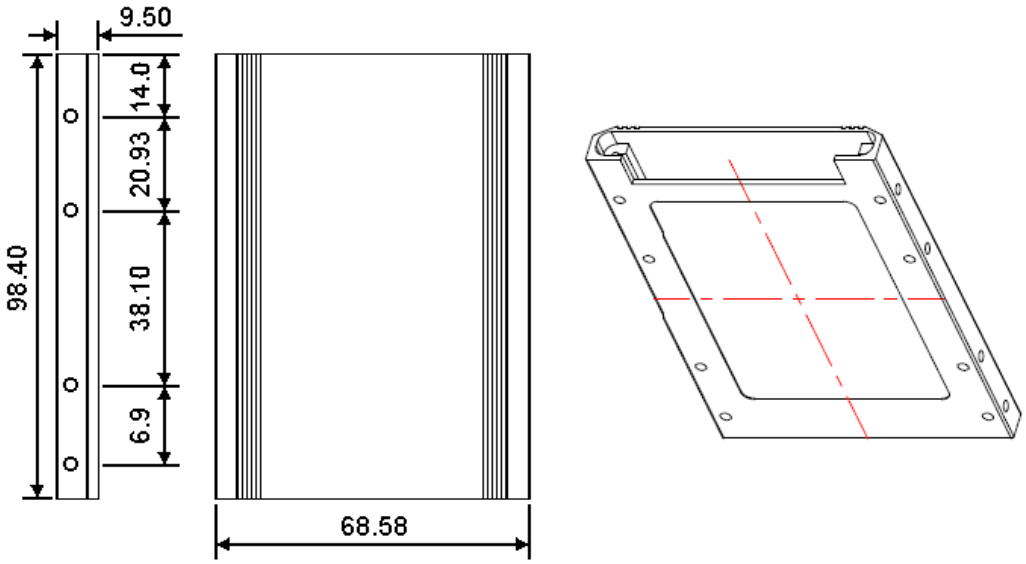
3.1. System Specification

Compatibility	ATAPI-4 Standard	
Flash Technology	NAND Type Flash Memory Base	
Form Factor	2.5inch or 1.8inch	
Connector Types	Standard 44pin male IDE connector	
Master/Slave	Setup By Jumper	
System Performance		
Data Transfer Mode	UDMA Mode 4	
Sequential Read	SLC Type	43Mbytes / sec Max.
	MLC Type	34Mbytes / sec Max.
Sequential Write	SLC Type	37Mbytes / sec Max.
	MLC Type	12Mbytes / sec Max.
Average Access Time	0.5ms	
Environmental Specification		
Standard Temperature	Operation	0ºC ~ +70ºC
	Non-operation	-20ºC ~ +80ºC
Wide Temperature	Operation	-40ºC ~ +85ºC
	Non-operation	-50ºC ~ +95ºC
Vibration	Operation max	20 G
	Non-operation max	20 G
Humidity	Operation max	5~95% non-condensing
	Non-operation max	5~95% non-condensing
Shock	Operation max	1500 G
	Non-operation max	1500 G
Reliability		
MTBF	> 2,000,000 hours	
Error Code Correction	4 bits ECC Code	
Data Reliability	< 1 non-recoverable error 10^{14} bits read	
Data Retention	10 years	
Power Consumption		
Power Voltage	+5V ± 10%	
Read Mode	57mA(Typ.)	
Write Mode	110mA(Typ.)	
Standby Mode	1.4mA(Typ.)	

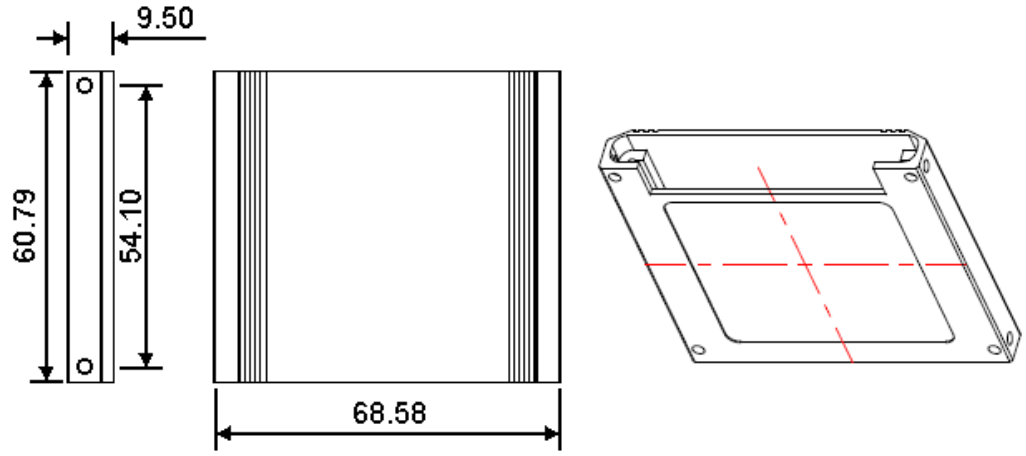
3.2. Block Diagram



3.3. Dimension



2.5 inch Form Factor



1.8 inch Form Factor

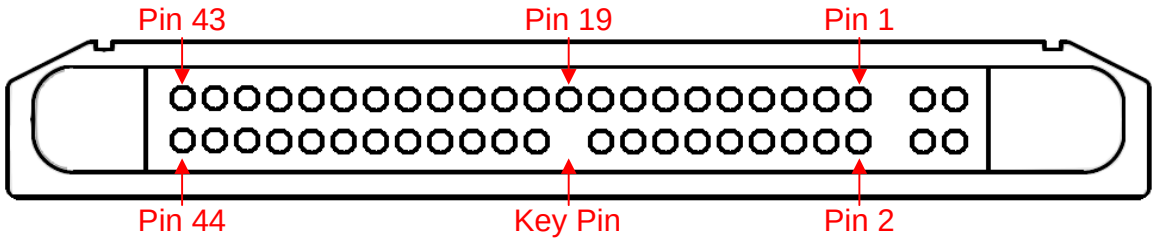
3.4. Capacity Specification

The specific capacities for the various models and the default number of heads, sectors and cylinders.

SLC/MLC Type				
Unformatted Capacity	Default Cylinder	Default Head	Default Sector	User Data Size
512MB	991	16	63	Depended on file management
1GB	1966	16	63	
2GB	3900	16	63	
4GB	7785	16	63	
8GB	15,538	16	63	
16GB	33114	15	63	
32GB	65535	15	63	

4 Pin Descriptions

4.1 Pin Layout



4.2 Pin Assignments

Pin #	Pin Name	Pin Type	Pin #	Pin Name	Pin Type
1	RESET-	I	2	Ground	Ground
3	DD7	I/O	4	DD8	I/O
5	DD6	I/O	6	DD9	I/O
7	DD5	I/O	8	DD10	I/O
9	DD4	I/O	10	DD11	I/O
11	DD3	I/O	12	DD12	I/O
13	DD2	I/O	14	DD13	I/O
15	DD1	I/O	16	DD14	I/O
17	DD0	I/O	18	DD15	I/O
19	Ground	Ground	20	Keypin	Power
21	DMARQ	O	22	Ground	Ground
23	DIOW-:STOP	I	24	Ground	Ground
25	DIOR-:HDMARDY-:HSTROBE	I	26	Ground	Ground
27	IORDY:DDMARDY-:DSTROBE	O	28	NC	--
29	DMACK-	I	30	Ground	Ground
31	INTRQ	O	32	IOCS16-	O
33	DA1	I	34	PDIAG-	I/O
35	DA0	I	36	DA2	I
37	CS0-	I	38	CS1-	I
39	DASP-	I/O	40	Ground	Ground
41	VCC	Power	42	VCC	Power
43	Ground	Ground	44	Ground	Ground

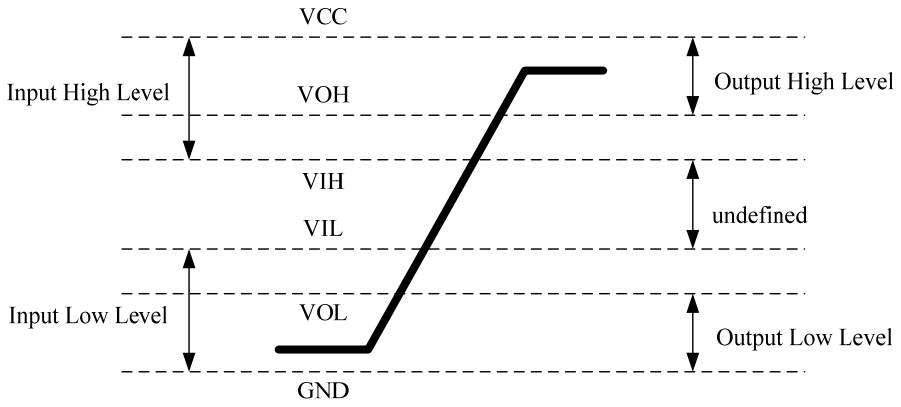
4.3 Signal Descriptions

Signal Name	I/O	Pin	Description
RESET-	I	1	This signal, referred to as hardware reset, shall be used by the host to reset the device.
DD[15:0]	I/O	03-18	This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers. Data transfers are 16-bits wide except for CFA device that implement 8-bit data transfers.
INTRQ	O	31	This signal is used by the selected device to interrupt the host system when interrupt pending is set.
DA[2:0]	I	33,35,36	This is the 3-bit binary coded address asserted by the host to access a register or data port in the device
CS0-,CS1-	I	37,38	These are the chip select signals from the host used to select the Command Block or Control Block registers. When DMACK- is asserted, CS0- and CS1- shall be negated and transfers shall be 16 bits wide.
IORDY	O	27	I/O channel ready
DDMARDY-			Flow control signal for Ultra DMA data-out bursts.
DSTROBE			The data-in strobe signal from the device for an Ultra DMA data-in burst.
-IOCS16	O	32	IOCS16- indicates to the host system that the 16-bit data port has been addressed and that the device is prepared to send or receive a 16-bit data word.
PDIAG-	I/O	34	PDIAG- shall be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics.
DASP-	I/O	39	This is a time-multiplexed signal that indicates that a device is active, or that Device 1 is present.
DIOR-	I	25	The strobe signal asserted by the host to read device registers or the Data port.
HDMARDY-			This signal is asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data-in bursts.
HSTROBE			The data-out strobe signal from the host for an Ultra DMA data-out burst.
DIOW-	I	23	The strobe signal asserted by the host to write device registers or the Data port.
STOP			Stop Ultra DMA data burst.
DMACK-	I	29	This signal shall be used by the host in response to DMARQ to initiate DMA transfers.
DMARQ	O	21	This signal, used for DMA data transfers between host and device, shall be asserted by the device when the device is ready to transfer data to or from the host.
Ground	GND	02,19,22, 24,26,30, 40,43,44	Ground
VCC	VCC	20,41,42	+5V DC Power

5 Electrical Specifications

5.1 DC Characters

Symbol	Parameter	Rating	Units
V_{CC}	Power Supply	-0.3 to 5.5	V
V_{IN}	Input Voltage	-0.3 to V_{CC} +0.3	V
V_{OUT}	Output Voltage	-0.3 to V_{CC} +0.3	V
V_{CCQ}	Power supply for host I/O and embedded regulator	-0.6 to 5.5	V
V_{IN_HOST}	Input voltage for host I/O	-0.3 to V_{CCQ} +0.3	V
V_{OUT_HOST}	Output voltage for host I/O	-0.3 to V_{CCQ} +0.3	V
T_{OPR-I}	Industrial temperature grade	-40° to +85°	℃
T_{OPR}	Commercial temperature grade	0° to +70°	℃
T_{STG}	Storage temperature	-55° to 150°	℃



Symbol	Parameter	MIN	TYP	MAX	Unit
Input low-voltage	V_{IL}			0.8	V
Input high-voltage	V_{IH}	2.0		5.0	V
Output low-voltage	V_{OL}	0		0.4	V
Output high-voltage	V_{OH}	2.6		3.6	V

5.2 AC Characters

5.2.1. True IDE PIO Mode Read/Write Timing

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min)[1]	600	383	240	180	120
t_1	Address Valid to HIOE/HIOW setup (min)	70	50	30	30	25
t_2	HIOE/HIOW (min)[1]	165	125	100	80	70
t_2	HIOE/HIOW (min) Register (8 bit)[1]	290	290	290	80	70
t_{2i}	HIOE/HIOW recovery time (min)[1]	-	-	-	70	25
t_3	HIOW data setup (min)	60	45	30	30	20
t_4	HIOW data hold (min)	30	20	15	10	10
t_5	HIOE data setup (min)	50	35	20	20	20
t_6	HIOE data hold (min)	5	5	5	5	5
t_{6Z}	HIOE data tristate (max)[2]	30	30	30	30	30
t_7	Address valid to IOCS16 assertion (max)[4]	90	50	40	n/a	n/a
t_8	Address valid to IOCS16 released (max)[4]	60	45	30	n/a	n/a
t_9	HIOE/HIOW to address valid hold	20	15	10	10	10
t_{RD}	Read Data Valid to IORDY active (min), if IORDY initially low after tA	0	0	0	0	0
t_A	IORDY Setup time[3]	35	35	35	35	35
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release (max)	5	5	5	5	5

Notes: All timings are in nanoseconds. The maximum load on IOCS16 is 1 LSTTL with a 50 pF (40pF below 120nsec Cycle Time) total load. All times are in nanoseconds. Minimum time from IORDY high to HIOE high is 0 nsec, but minimum HIOE width shall still be met.

(1) t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation can lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the device's identify device data.

(2) This parameter specifies the time from the negation edge of HIOE to the time that the data bus is no longer driven by the device.

(3) The delay from the activation of HIOE or HIOW until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle can be completed. If the device is not driving IORDY negated at t_A after the activation of HIOE or HIOW, then t5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of HIOE or HIOW, then t_{RD} shall be met and t5 is not applicable.

(4) t7 and t8 apply only to modes 0, 1 and 2. For other modes, this signal is not valid.

(5) IORDY is not supported in this mode.

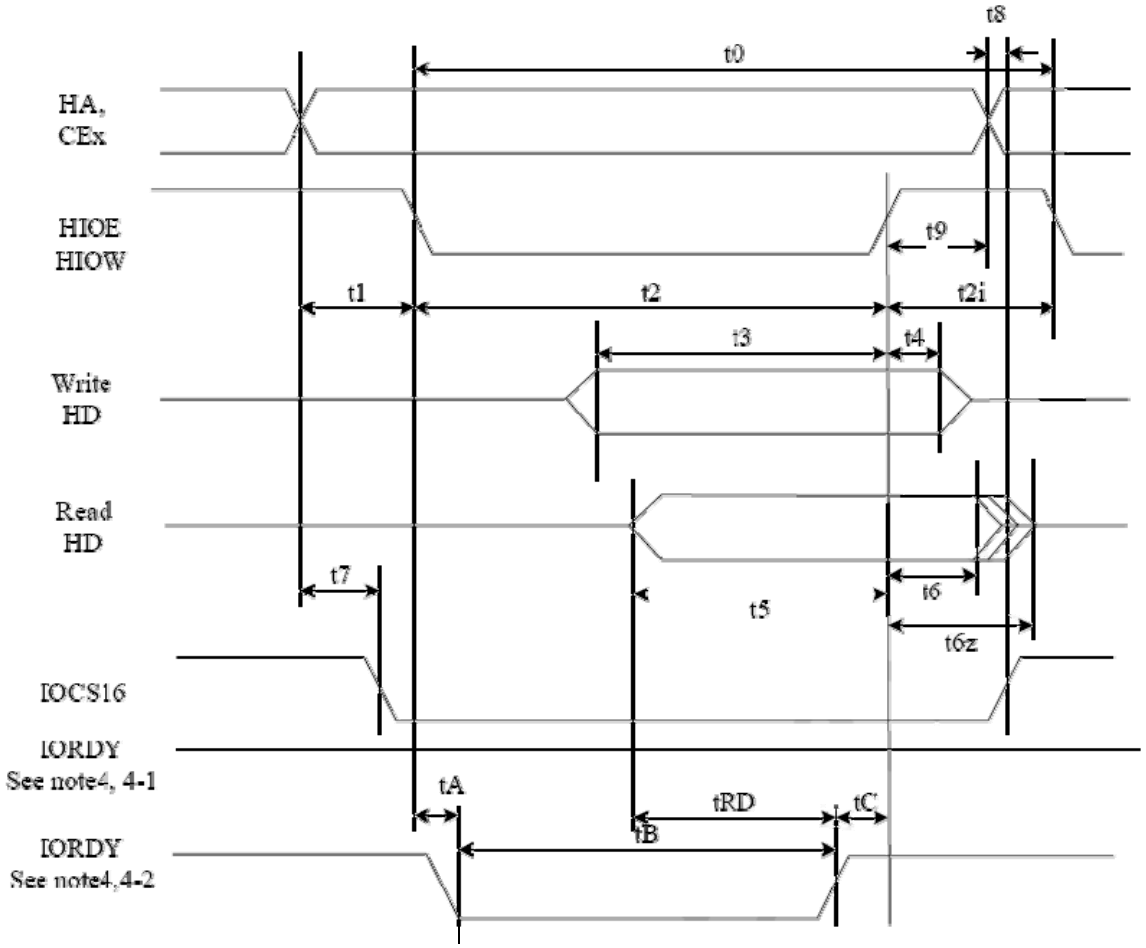


Figure 1 True IDE Mode Read/Write Timing Diagram

Notes:

(1) Device address consists of CE0, CE1, and HA[2:0]

(2) Data consists of HD[15:00] (16-bit) or HD[7:0] (8 bit)

(3) IOCS16 is shown for PIO modes 0, 1 and 2. For other modes, this signal is ignored.

(4) The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of HIOE or HIOW. The assertion and negation of IORDY is described in the following three cases:

(4-1) Device never negates IORDY: No wait is generated.

(4-2) Device drives IORDY low before t_A: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and HIOE is asserted, the device shall place read data on D15-D00 for t_{RD} before causing IORDY to be asserted.

5.2.2. True IDE Multiword DMA Mode Read/Write Timing

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Note
t_O	Cycle time (min)	480	150	120	100	80	1
t_D	HIOE / HIOW asserted width (min)	215	80	70	65	55	1
t_E	HIOE data access (max)	150	60	50	50	45	
t_F	HIOE data hold (min)	5	5	5	5	5	
t_G	HIOE/HIOW data setup (min)	100	30	20	15	10	
t_H	HIOW data hold (min)	20	15	10	5	5	
t_I	DMACK(HREG) to HIOE/HIOW setup (min)	0	0	0	0	0	
t_J	HIOE / HIOW to -DMACK hold (min)	20	5	5	5	5	
t_{KR}	HIOE negated width (min)	50	50	25	25	20	1
t_{KW}	HIOW negated width (min)	215	50	25	25	20	1
t_{LR}	HIOE to DMARQ delay (max)	120	40	35	35	35	
t_{LW}	HIOW to DMARQ delay (max)	40	40	35	35	35	
t_M	CEx valid to HIOE / HIOW	50	30	25	10	5	
t_N	CEx hold	15	10	10	10	10	

Notes: t_0 is the minimum total cycle time and t_D is the minimum command active time, while t_{KR} and t_{KW} are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_{KR}, and t_{KW} shall be met. The minimum total cycle time requirement is greater than the sum of t_D and t_{KR} or t_{KW} for input and output cycles respectively. This means a host implementation can lengthen either or both of t_D and either of t_{KR}, and t_{KW} as needed to ensure that t_0 is equal to or greater than the value reported in the device's identify device data. A device implementation shall support any legal host implementation.

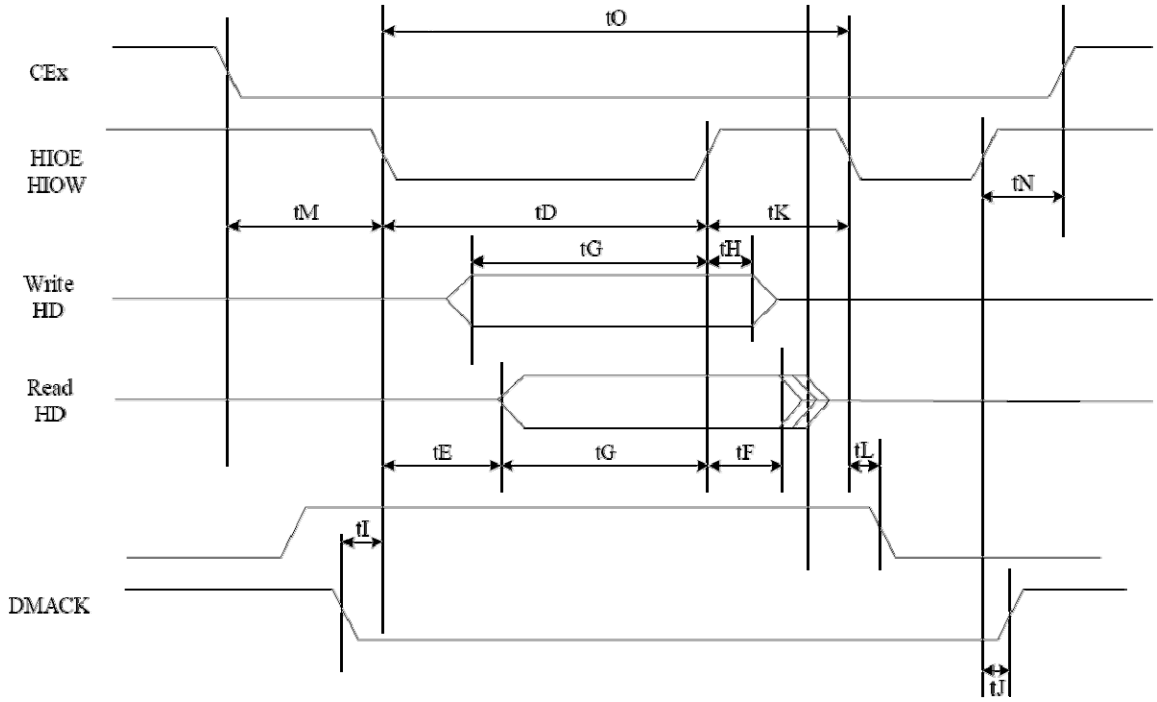


Figure 2 True IDE Multiword DMA Mode Read/Write Timing Diagram

Notes:

(1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of a DMA transfer cycle to suspend the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.

(2) This signal may be negated by the host to suspend the DMA transfer in progress.

5.2.3. Ultra DMA Mode Read/Write Timing

5.2.3.1. Ultra DMA Signal

Signal	Type	TRUE IDE MODE UDMA
DMARQ	Output	DMARQ
HREG	Input	-DMACK
HIOW	Input	STOP[1]
HIOE	Input	-HDMARDY[1,2] HSTROBE(W)[1,3,4]
IORDY	Output	-DDMARDY(W)[1,3] DSTROBE(R)[1,2,4]
HD[15:00]	Bidir	D[15:00]
HA[10:00]	Input	A[02:00][5]
CSEL	Input	-CSEL
HIRQ	Output	INTRQ
CE1 CE2	Input	-CS0 -CS1

Notes:

(1) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst.

(2) The UDMA interpretation of this signal is valid only during and Ultra DMA data burst during a DMA Read command.

(3) The UDMA interpretation of this signal is valid only during an Ultra DMA data burst during a DMA Write command.

(4) The HSTROBE and DSTROBE signals are active on both the rising and the falling edge.

(5) Address lines 03 through 10 are not used in True IDE mode.

5.2.3.2. Ultra DMA Data Burst Timing Requirements

Name	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Measure Location[2]
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{2CYCTYP}$	240		160		120		90		60		Sender
t_{CYC}	112		73		54		39		25		Note3
t_{2CYC}	230		153		115		86		57		Sender
t_{DS}	15.0		10.0		7.0		7.0		5.0		Recipient
t_{DH}	5.0		5.0		5.0		5.0		5.0		Recipient
t_{DVS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{DVH}	6.2		6.2		6.2		6.2		6.2		Sender
t_{CS}	15.0		10.0		7.0		7.0		5.0		Device
t_{CH}	5.0		5.0		5.0		5.0		5.0		Device
t_{CVS}	70.0		48.0		31.0		20.0		6.7		Host
t_{CVH}	6.2		6.2		6.2		6.2		6.2		Host
t_{ZFS}	0		0		0		0		0		Device
t_{DZFS}	70.0		48.0		31.0		20.0		6.7		Sender
t_{FS}		230		200		170		130		120	Device
t_{LI}	0	150	0	150	0	150	0	100	0	100	Note4
t_{MLI}	20		20		20		20		20		Host
t_{UI}	0		0		0		0		0		Host
t_{AZ}		10		10		10		10		10	Note5
t_{ZAH}	20		20		20		20		20		Host
t_{ZAD}	0		0		0		0		0		Device
t_{ENV}	20	70	20	70	20	70	20	55	20	55	Host
t_{RFS}		75		70		60		60		60	Sender
t_{RP}	160		125		100		100		100		Recipient
t_{IORDYZ}		20		20		20		20		20	Device
t_{ZIORDY}	0		0		0		0		0		Device
t_{ACK}	20		20		20		20		20		Host
t_{SS}	50		50		50		50		50		Sender

Notes: All Timings in ns

(1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

(2) All signal transitions for a timing parameter shall be measured at the connector specified in the measurement location column. For example, in the case of t_{RFS}, both STROBE and -DMARDY transitions are measured at the sender connector.

(3) The parameter t_{CYC} shall be measured at the recipient's connector farthest from the sender.

(4) The parameter t_{LI} shall be measured at the connector of the sender or recipient that is responding to an incoming transition from the recipient or sender respectively. Both the incoming signal and the outgoing response shall be measured at the same connector.

(5) The parameter t_{AZ} shall be measured at the connector of the sender or recipient that is driving the bus but must release the bus to allow for a bus turnaround.

(6) See the AC Timing requirements in 5.2.3.5.Ultra DMA AC Signal Requirements.

5.2.3.3. Ultra DMA Data Burst Timing Descriptions

Name	Comment	Notes
$t_{2CYCTYP}$	Typical sustained average two cycle time	
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge next falling edge of STROBE)	
t_{DS}	Data setup time at recipient (from data valid until STROBE edge)	2
t_{DH}	Data hold time at recipient (from STROBE edge until data may become invalid)	2
t_{DVS}	Data valid setup time at sender (from data valid until STROBE edge)	3
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	3
t_{CS}	CRC word setup time at device	2
t_{CH}	CRC word hold time device	2
t_{CVS}	CRC word valid setup time at host (from CRC valid until -DMACK negation)	3
t_{CVH}	CRC word valid hold time at sender (from -DMACK negation until CRC may become invalid)	3
t_{ZFS}	Time from STROBE output released-to-driving until the first transition of critical timing.	
t_{DZFS}	Time from data output released-to-driving until the first transition of critical timing.	
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	
t_{LI}	Limited interlock time	1
t_{MLI}	Interlock time with minimum	1
t_{UI}	Unlimited interlock time	1
t_{AZ}	Maximum time allowed for output drivers to release (from asserted or negated)	
t_{ZAH}	Minimum delay time required for output	
t_{ZAD}	drivers to assert or negate (from released)	
t_{ENV}	Envelope time (from -DMACK to STOP and -HDMARDY during data in burst initiation and from DMACK to STOP during data out burst initiation)	
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of -DMARDY)	
t_{RP}	Ready-to-pause time (that recipient shall wait to pause after negating -DMARDY)	
t_{IORDYZ}	Maximum time before releasing IORDY	
t_{ZIORDY}	Minimum time before driving IORDY	4
t_{ACK}	Setup and hold times for -DMACK (before assertion or negation)	
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	

Notes:

(1) The parameters t_{UI}, t_{MLI} (in 5.2.3.9: Ultra DMA Data-In Burst Device Termination Timing and 5.2.3.10: Ultra DMA Data-In Burst Host Termination Timing), and t_{LI} indicate sender-to-recipient or recipient-to-sender interlocks, i.e., one agent (either sender or recipient) is waiting for the other agent to respond with a signal before proceeding. t_{UI} is an unlimited interlock that has no maximum time value. t_{MLI} is a limited time-out that has a defined minimum. t_{LI} is a limited time-out that has a defined maximum.

(2) 80-conductor cabling (see ATA specification :Annex A) shall be required in order to meet setup (t_{DS}, t_{CS}) and hold (t_{DH}, t_{CH}) times in modes greater than 2.

(3) Timing for t_{DVS}, t_{DVH}, t_{CVS} and t_{CVH} shall be met for lumped capacitive loads of 15 and 40 pF at the connector where the Data and STROBE signals have the same capacitive load value. Due to reflections on the cable, these timing measurements are not valid in a normally functioning system.

(4) For all timing modes the parameter t_{ZIORDY} may be greater than t_{ENV} due to the fact that the host has a pull-up on IORDY- giving it a known state when released.

5.2.3.4. Ultra DMA Data Burst Timing Requirements

Name	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
t_{DSIC}	14.7		9.7		6.8		6.8		4.8	
t_{DHIC}	4.8		4.8		4.8		4.8		4.8	
t_{DVSIC}	72.9		50.9		33.9		22.6		9.5	
t_{DVHIC}	9.0		9.0		9.0		9.0		9.0	
t_{DSIC}	Recipient IC data setup time (from data valid until STROBE edge) (see note 2)									
t_{DHIC}	Recipient IC data hold time (from STROBE edge until data may become invalid) (see note 2)									
t_{DVSIC}	Sender IC data valid setup time (from data valid until STROBE edge) (see note 3)									
t_{DVHIC}	Sender IC data valid hold time (from STROBE edge until data may become invalid) (see note 3)									

Notes:

(1) All timing measurement switching points (low to high and high to low) shall be taken at 1.5 V.

(2) The correct data value shall be captured by the recipient given input data with a slew rate of 0.4 V/ns rising and falling and the input STROBE with a slew rate of 0.4 V/ns rising and falling at t_{DSIC} and t_{DHIC} timing (as measured through 1.5 V).

(3) The parameters t_{DVSIC} and t_{DVHIC} shall be met for lumped capacitive loads of 15 and 40 pF at the IC where all signals have the same capacitive load value. Noise that may couple onto the output signals from external sources has not been included in these values.

5.2.3.5. Ultra DMA AC Signal Requirements

Name	Comment	Min [V/ns]	Max [V/ns]	Notes
SRISE	Rising Edge Slew Rate for any signal		1.25	1
SFALL	Falling Edge Slew Rate for any signal		1.25	1

Notes:

(1) The sender shall be tested while driving an 18 inch long, 80 conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has not trace, cable or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and one half inch or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within one half inch of the connector.

The test load and test points should then be soldered directly to the exposed source side connectors. The test loads consist of a 15 pF or a 40 pF, 5%, 0.08 inch by 0.05 inch surface mount or smaller size capacitor from the test point to ground. Slew rates shall be met for both capacitor values.

Measurements shall be taken at the test point using a <1 pF, >100 Kohm, 1 Ghz or faster probe and a 500 MHz or faster oscilloscope. The average rate shall be measured from 20% to 80% of the settled VOH level with data transitions at least 120 nsec apart. The settled VOH level shall be measured as the average output high level under the defined testing conditions from 100 nsec after 80% of a rising edge until 20% of the subsequent falling edge.

5.2.3.6. Ultra DMA Data-In Burst Initiation Timing

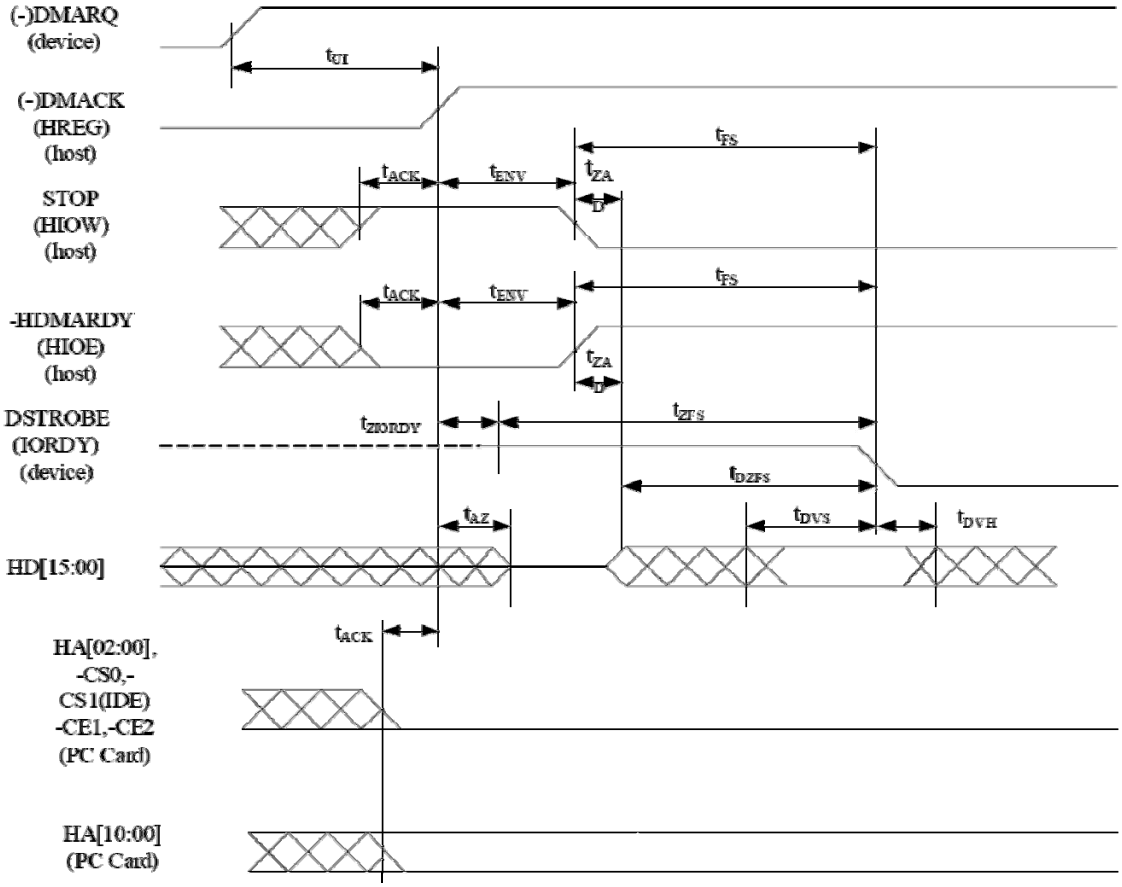


Figure 3 Ultra DMA Data-In Burst Initiation Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

(1) The definitions for the IORDY:-DDMARDY:DSTROBE, -IORD:-HDMARDY:HSTROBE, and -IOWR:STOP signal lines are not in effect until DMARQ and -DMACK are asserted. HA[02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signals. The Bus polarity of (-) DMACK and (-) DMARQ are dependent on interface mode active.

5.2.3.7. Sustained Ultra DMA Data-In Burst Timing

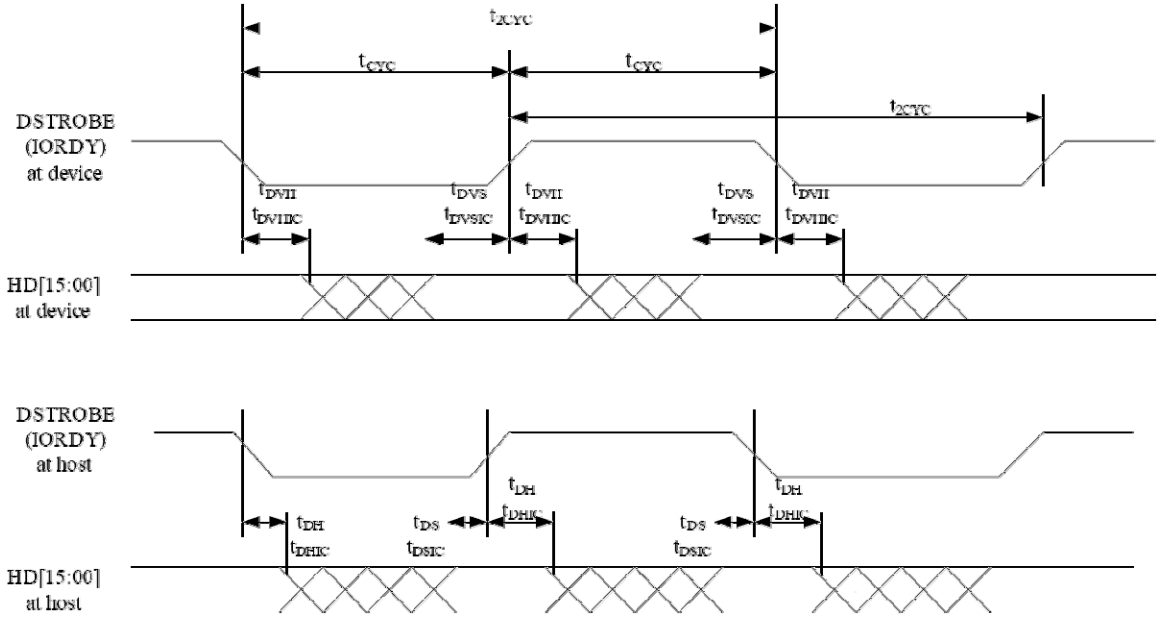


Figure 4 Sustained Ultra DMA Data-In Burst Timing Diagram

Notes: HD[15:00] and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

5.2.3.8. Ultra DMA Data-In Burst Host Pause Timing

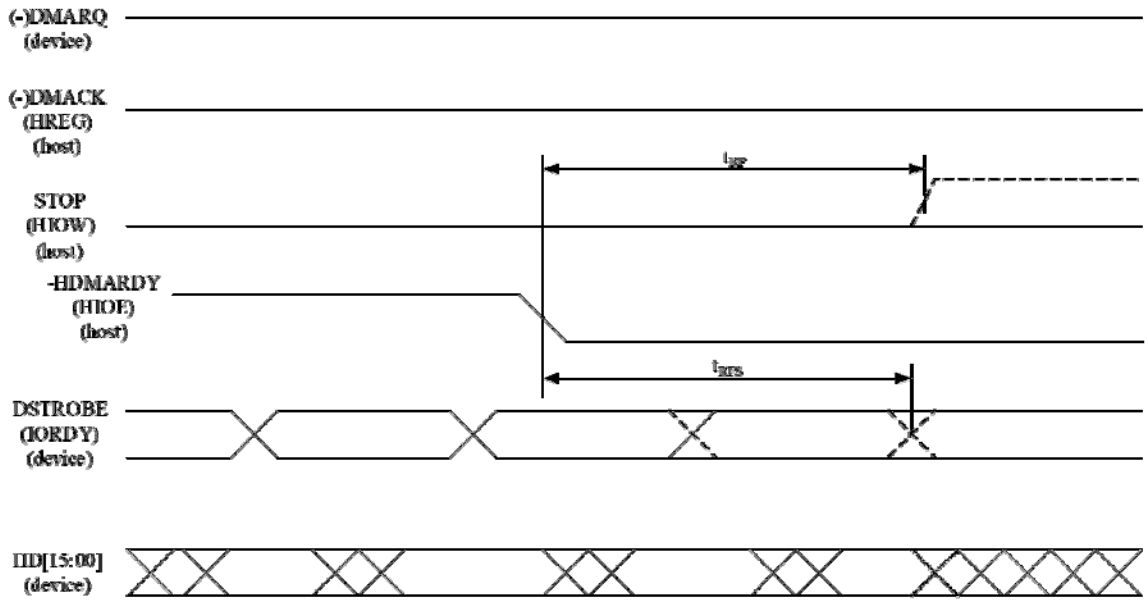


Figure 5 Ultra DMA Data-In Burst Host Pause Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

(1) The host may assert STOP to request termination of the Ultra DMA data burst no sooner than tRP after -HDMARDY is negated.

(2) After negating -HDMARDY, the host may receive zero, one, two, or three more data words from the device.

(3) The bus polarity of the (-) DMARQ and (-)DMACK signals is dependent on the active interface mode.

5.2.3.9. Ultra DMA Data-In Burst Device Termination Timing

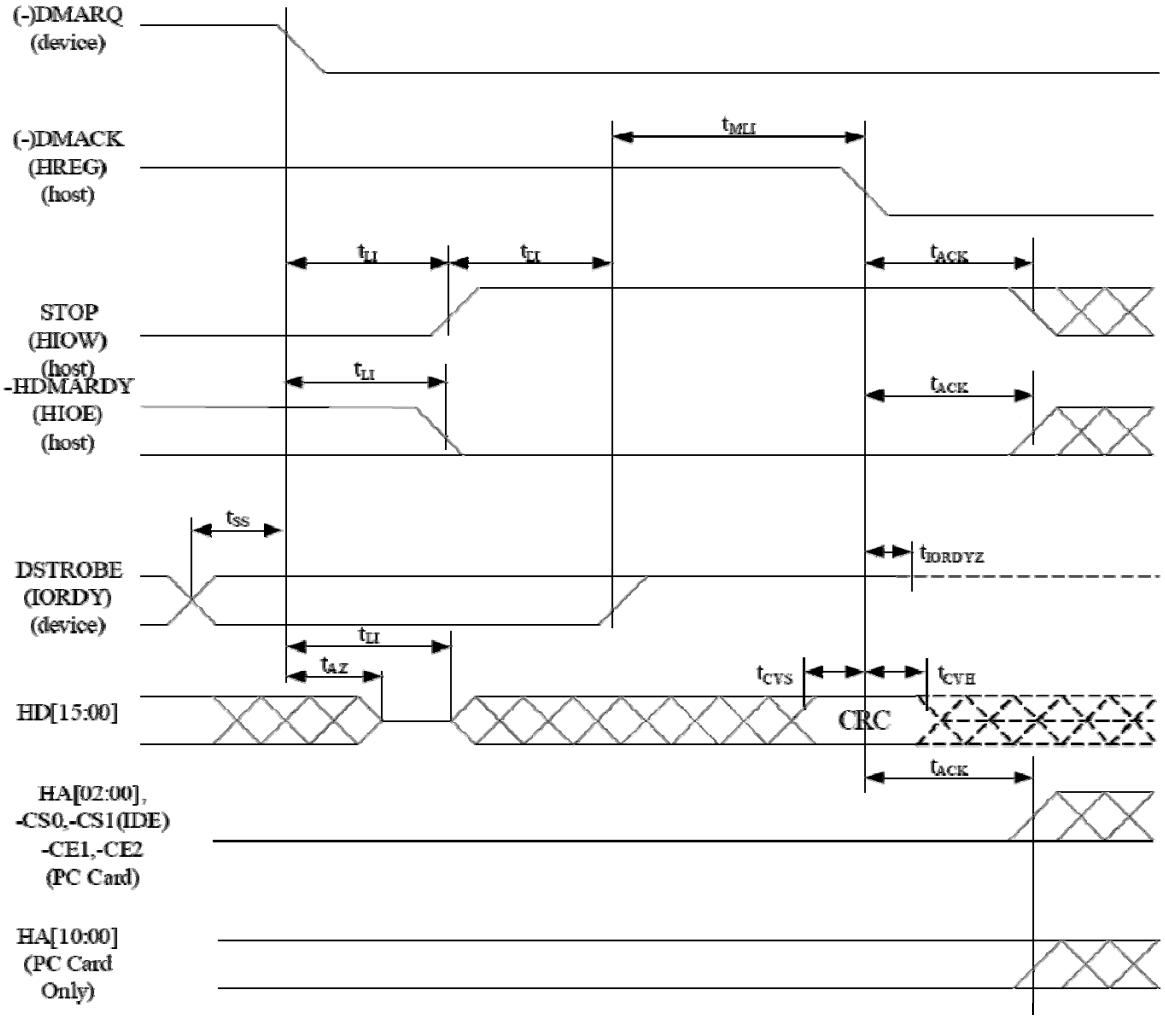


Figure 6 Ultra DMA Data-In Burst Device Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK are dependent on the active interface mode.

5.2.3.10. Ultra DMA Data-In Burst Host Termination Timing

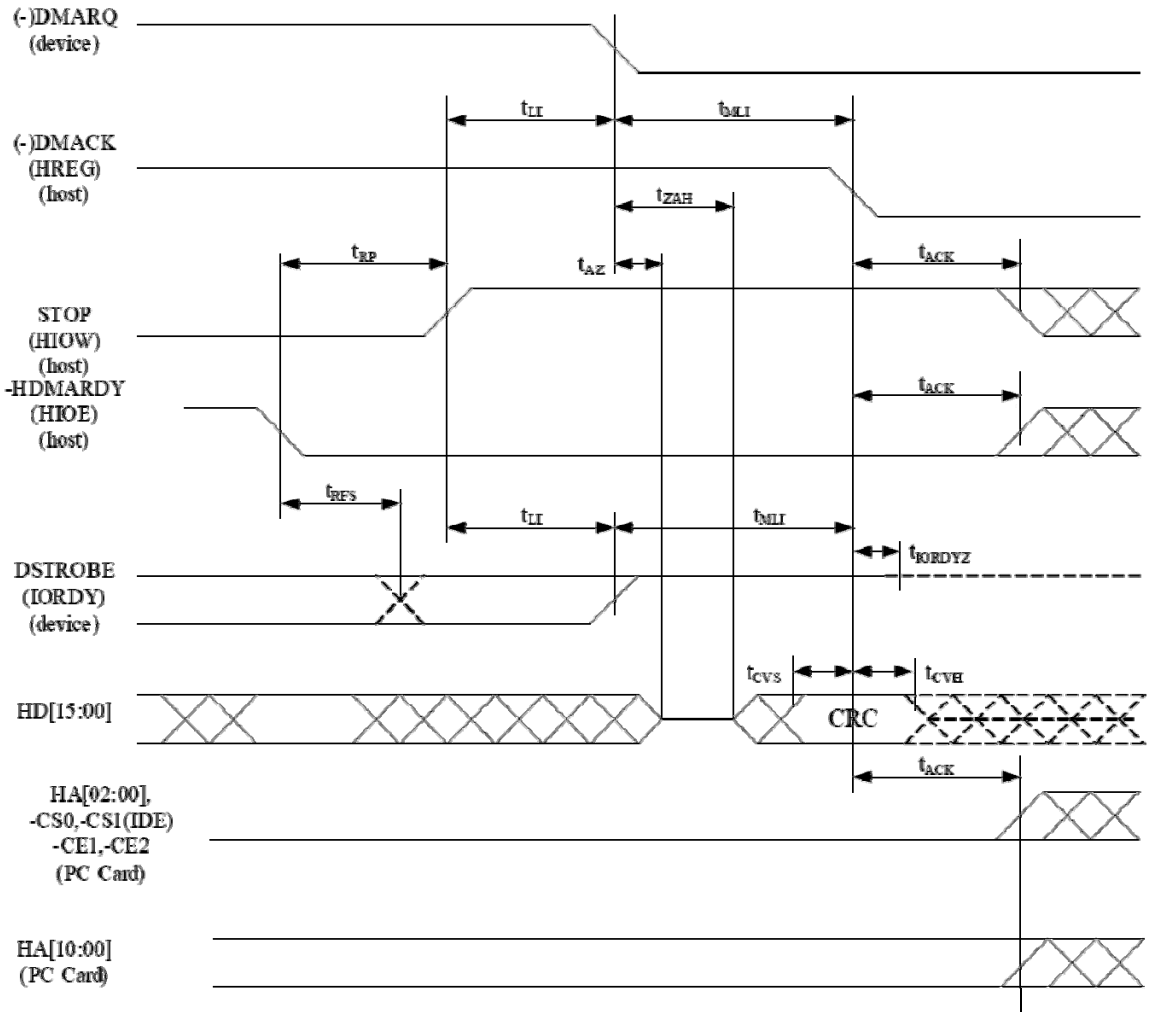


Figure 7 Ultra DMA Data-In Burst Host Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, HDMARDY, and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA [02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA [10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

5.2.3.11. Ultra DMA Data-Out Burst Initiation Timing

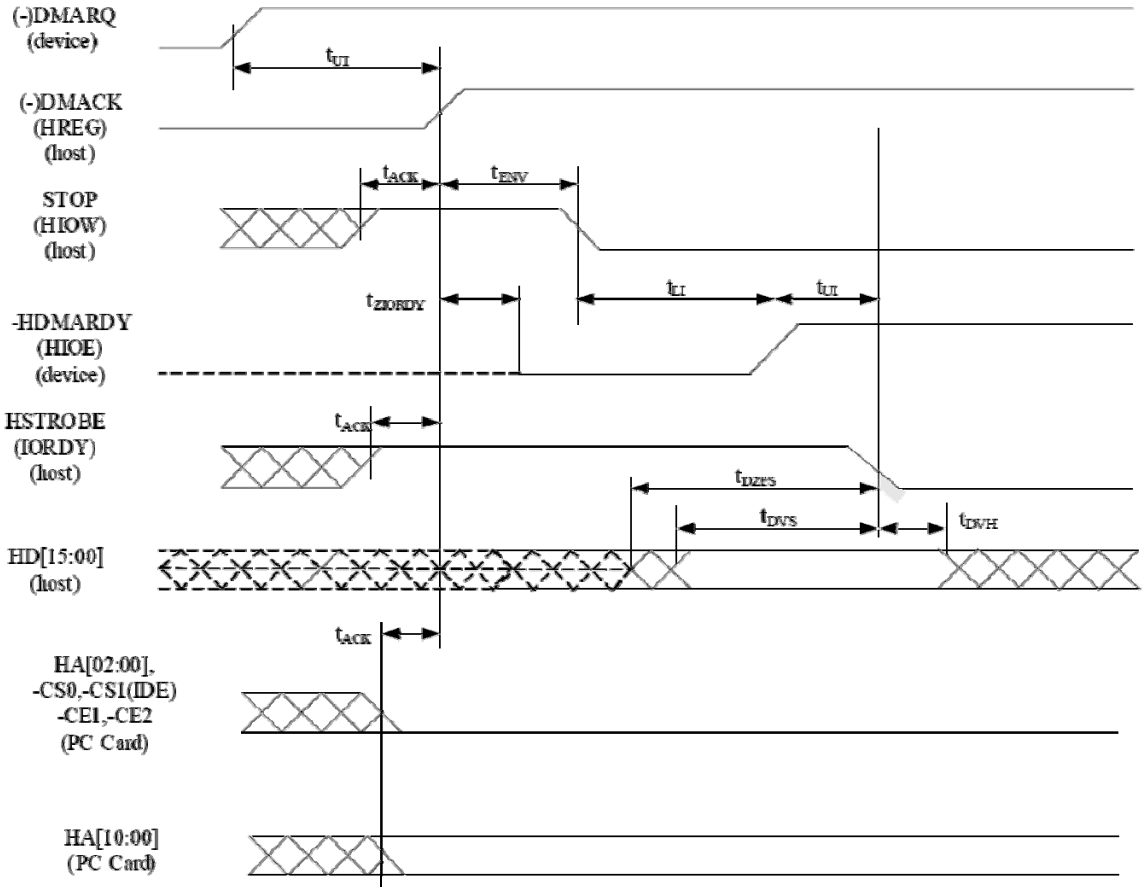


Figure 8 Ultra DMA Data-Out Burst Initiation Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are not in effect until DMARQ and DMACK are asserted. HA [02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA [10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

5.2.3.12. Sustained Ultra DMA Data-Out Burst Timing

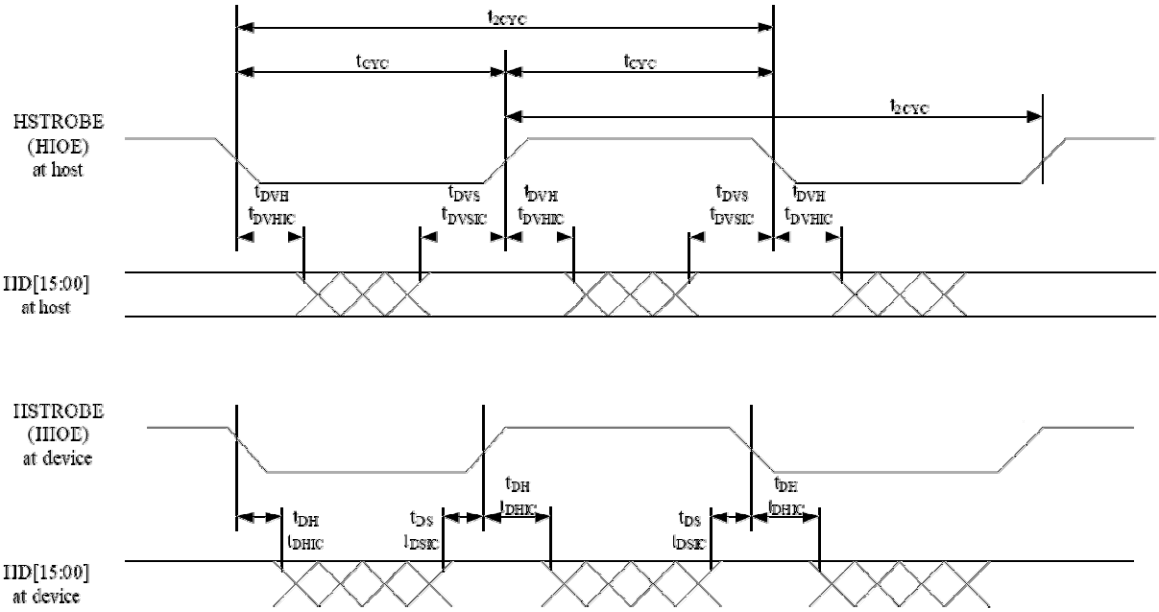


Figure 9 Sustained Ultra DMA Data-Out Burst Timing Diagram

Notes: Data (HD[15:00]) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

5.2.3.13. Ultra DMA Data-Out Burst Device Pause Timing

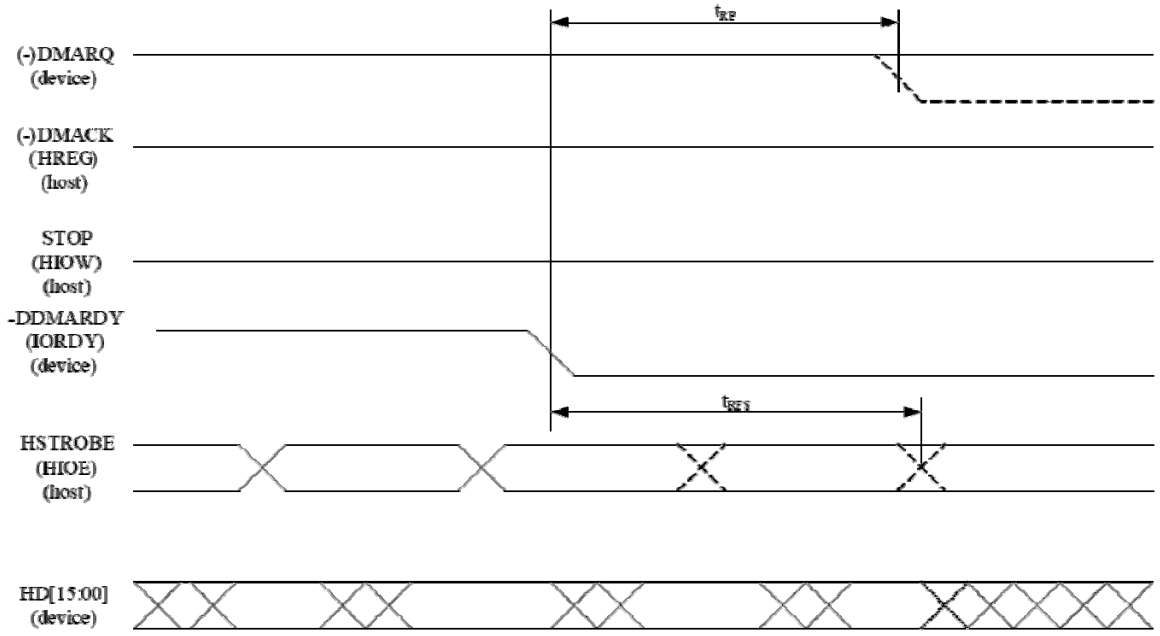


Figure 10 Ultra DMA Data-Out Burst Device Pause Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes:

(1) The device may negate DMARQ to request termination of the Ultra DMA data burst no sooner than t_{RP} after -DDMARDY is negated.

(2) After negating -DDMARDY, the device may receive zero, one, two, or three more data words from the host.

(3) The bus polarity of DMARQ and DMACK depend on the active interface mode.

5.2.3.14. Ultra DMA Data-Out Burst Device Termination Timing

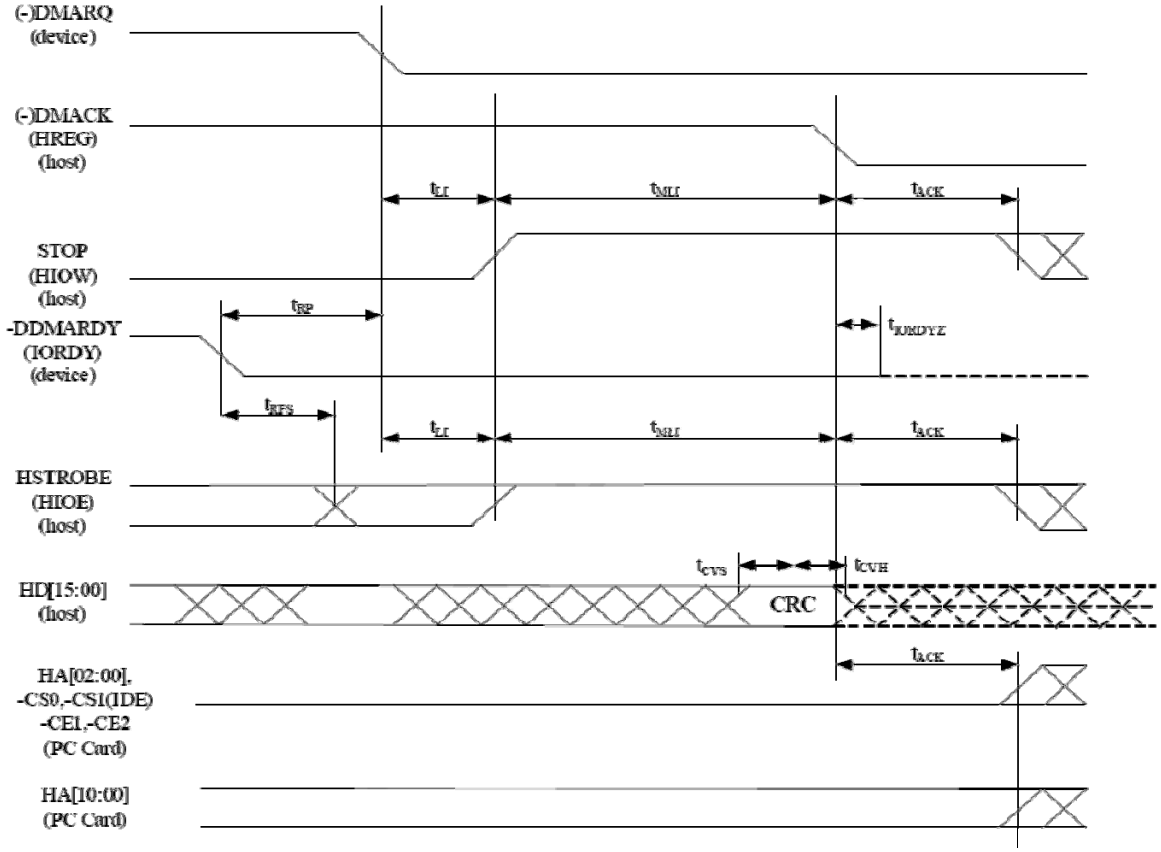


Figure 11 Ultra DMA Data-Out Burst Device Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[00:02], -CS0 & -CS1 are True IDE mode signal definitions. HA[00:10], -CE1 and -CE2 are PC Card mode signals. The bus polarity of DMARQ and DMACK depend on the active interface mode.

5.2.3.15. Ultra DMA Data-Out Burst Host Termination Timing

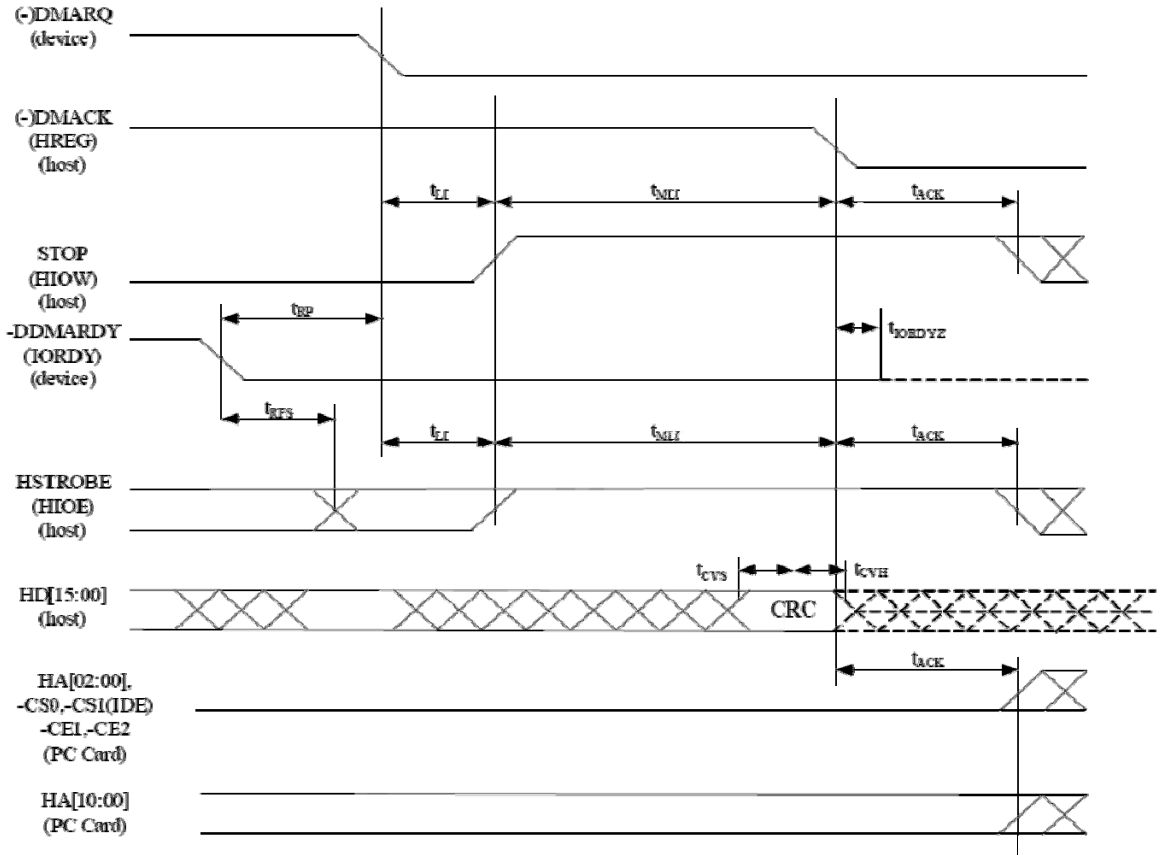


Figure 12 Ultra DMA Data-Out Burst Host Termination Timing Diagram

ALL WAVEFORMS IN THIS DIAGRAM ARE SHOWN WITH THE ASSERTED STATE HIGH. NEGATIVE TRUE SIGNALS APPEAR INVERTED ON THE BUS RELATIVE TO THE DIAGRAM.

Notes: The definitions for the STOP, DDMARDY, and HSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated. HA[02:00], -CS0 & -CS1 are True IDE mode signal definitions. HA[10:00], -CE1 and -CE2 are PC Card mode signal definitions. The bus polarity of DMARQ and DMACK depend on the active interface mode.

6 Command Descriptions

6.1 Command Support

Command	Code	FR	SC	SN	CY	DH	LBA
Check Power Mode	E5 or 98h	–	–	–	–	Y	–
Execute Drive Diagnostic	90h	–	–	–	–	Y	–
Erase Sector	C0h	–	Y	Y	Y	Y	Y
Format Track	50h	–	Y	–	Y	Y	Y
Identify Device	Ech	–	–	–	–	Y	–
Idle	E3h or 97h	–	Y	–	–	Y	–
Idle Immediate	E1h or 95h	–	–	–	–	Y	–
Initialize Drive Parameters	91h	–	Y	–	–	Y	–
NOP	00h	–	–	–	–	Y	–
Read Buffer	E4h	–	–	–	–	Y	–
Read DMA	C8h	–	Y	Y	Y	Y	Y
Read Multiple	C4h	–	Y	Y	Y	Y	Y
Read Sector(s)	20h or 21h	–	Y	Y	Y	Y	Y
Read Verify Sector(s)	40h or 41h	–	Y	Y	Y	Y	Y
Recalibrate	1Xh	–	–	–	–	Y	–
Request Sense	03h	–	–	–	–	Y	–
Security Disable Password	F6h	–	–	–	–	Y	–
Security Erase Prepare	F3h	–	–	–	–	Y	–
Security Erase Unit	F4h	–	–	–	–	Y	–
Security Freeze Lock	F5h	–	–	–	–	Y	–
Security Set Password	F1h	–	–	–	–	Y	–
Security Unlock	F2h	–	–	–	–	Y	–
Seek	7Xh	–	–	Y	Y	Y	Y
Set Feature	EFh	Y	–	–	–	Y	–
Set Multiple Mode	C6h	–	Y	–	–	Y	–
Set Sleep Mode	E6h or 99h	–	–	–	–	Y	–
Standby	E2 or 96h	–	–	–	–	Y	–
Standby Immediate	E0 or 94h	–	–	–	–	Y	–
Translate Sector	87h	–	Y	Y	Y	Y	Y
Wear Level	F5h	–	–	–	–	Y	–
Write Buffer	E8h	–	–	–	–	Y	–
Write DMA	CAh	–	Y	Y	Y	Y	Y
Write Multiple	C5h	–	Y	Y	Y	Y	Y
Write Multiple w/o Erase	CDh	–	Y	Y	Y	Y	Y
Write Sector(s)	30h or 31h	–	Y	Y	Y	Y	Y
Write Sector(s) w/o Erase	38h	–	Y	Y	Y	Y	Y
Write Verify	3Ch	–	Y	Y	Y	Y	Y

Note:

1. *FR: Feature Register*
   SC: Sector Count register
   SN: Sector Number register
   CY: Cylinder Low/High register
   DR: Drive bit of Drive/Head register
   HD: Head No. (bit0-bit3) of Drive/Head register
   LBA: Logical Block Address Mode Supported.
2. *Y: Set up*
   —: Not set up

6.2 SMART Command Support

IFD series supports SMART command set and define some vendor specific data to report spare/bad block number in each memory management unit. Users can get the data by "Read Data" command.

SMART Feature Register Values			
D0h	Read Data	D4h	Execute OFF-LINE Immediate
D1h	Read Attribute Threshold	D8h	Enable SMART Operations
D2h	Enable/Disable Autosave	D9h	Disable SMART Operations
D3h	Save Attribute Values	DAh	Return Status

Notes: If reserved size below the Threshold, the status can be read from Cylinder register by Return Status command (DAh).

SMART Data Structure (READ DATA (D0h))

BYTE	F / V	Decription
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396	V	Number of MU in device (0~n)
397+(n*6)	V	MU number
398+(n*6)	V	MU data block
400+(n*6)	V	MU spare block
401+(n*6)	V	Init. Bad block
402+(n*6)	V	Run time Bad block information
511	V	Data structure checksum

Notes:
F = the content of the byte is fixed and does not change.
V = the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.
X = the content of the byte is vendor specific and may be fixed or variable.
R = the content of the byte is reserved and shall be zero.
N = Nth Management Unit
** 4 Byte value : [MSB] [2] [1] [LSB]*

6.3 ID Table Information

Word Address	Default value	Total Bytes	Data Field Type information
0	044Ah	2	General configuration
1	XXXXh	2	Default number of cylinders
2	0000h	2	Reserved
3	00XXh	2	Default number of heads
4	0000h	2	Obsolete
5	0240h	2	Obsolete
6	XXXXh	2	Default number of sectors per track
7-8	XXXXh	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXXh	20	Serial number in ASCII (Right Justified)
20	0002h	2	Obsolete
21	0002h	2	Obsolete
22	0004h	2	Number of ECC bytes passed on Read/Write Long Commands
23-26	XXXXh	8	Firmware revision in ASCII. Big Endean Byte Order in Word
27-46	XXXXh	40	Model number in ASCII (Left Justified) Big Endean Byte Order in Word
47	8001h	2	Maximum number of sectors on Read/Write Multiple command
48	0000h	2	Reserved
49	0300h	2	Capabilities
50	0000h	2	Reserved
51	0200h	2	PIO data transfer cycle timing mode
52	0000h	2	Obsolete
53	0007h	2	Field validity
54	XXXXh	2	Current numbers of cylinders
55	XXXXh	2	Current numbers of heads
56	XXXXh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in sectors (LBAs)(Word57=LSW , Word58=MSW)
59	0101h	2	Multiple sector setting
60-61	XXXXh	4	Total number of sectors addressable in LBA Mode
62	0000h	2	Reserved
63	0407h	2	Multiword DMA transfer. In PCMCIA mode this value shall be oh
64	0003h	2	Advanced PIO modes supported
65	0078h	2	Minimum Multiword DMA transfer cycle time per word.
66	0078h	2	Recommended Multiword DMA transfer cycle time.
67	0078h	2	Minimum PIO transfer cycle time without flow control
68	0078h	2	Minimum PIO transfer cycle time with lORDY flow control
69-79	0000h	20	Reserved
80	0010h	2	Major version number
81	0000h	2	Minor version number
82	7008h	2	Command sets supported 0
83	400Ch	2	Command sets supported 1
84	4002h	2	Command sets supported 2
85	0001h	2	Command sets Enable 0
86	0000h	2	Command sets Enable 1
87	0002h	2	Command sets Enable 2
88	001Fh	2	True IDE Ultra DMA Mode Supported and Selected (UDMA0~4)

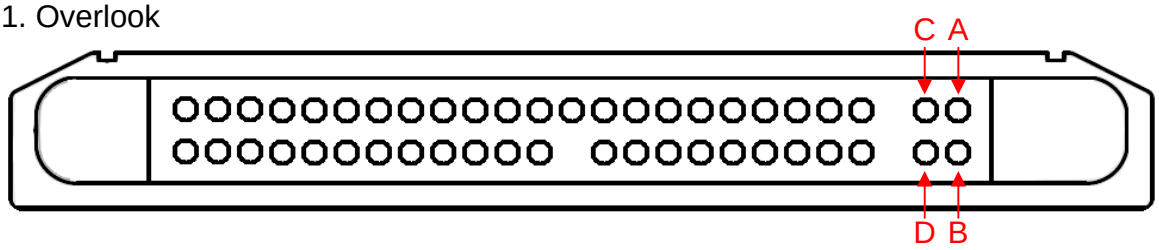
89	0000h	2	Time required for Security erase unit completion
90	0000h	2	Time required for Enhanced security erase unit completion
91	0000h	2	Current Advanced power manage mentvalue
92-127	0000h	72	Reserved
128	0000h	2	Security status
129-159	0000h	64	vendor unique bytes
160	81F4h	2	Power requirement description
161	0000h	2	Reserved for assignment by the CFA
162	0000h	2	Key management schemes supported
163	0492h	2	CF Advanced True IDE Timing Mode Capability and Setting
164	001Bh	2	CF Advanced PCMCIA I/O and Memory Timing Mode Capability and set
165-175	0000h	22	80ns cycle in memory and IO mode
176-255	0000h	140	Reserved for assignment by the CFA

Notes:
Word 1: Default number of cylinders .
Word 3: Default number of heads .
Word 6: Default number of sectors per track .
Word 10~19: Serial number in ASCII .
Word 23~26: Firmware revision in ASCII.
Word 27~26: Model number in ASCII

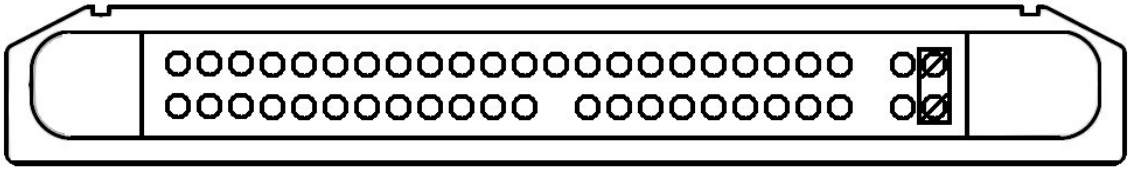
7 Hardware Function

7.1. Master/Slave Setup

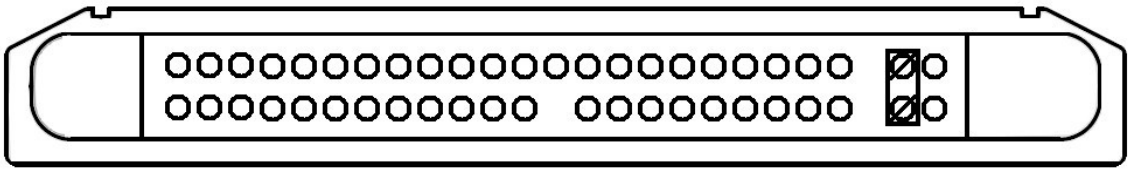
1. Overlook



2. Master Mode



3. Slave Mode



8 Ordering Information

8.1 2.5 inch Form Factor

Capacity	Standard Temp.	Wide Temp.
128MB[2]	IFD-25SI128MBCFX[1]	IFD-25SI128MBIFX[1]
256MB	IFD-25SI256MBCFX[1]	IFD-25SI256MBIFX[1]
512MB	IFD-25SI512MBCFX[1]	IFD-25SI512MBIFX[1]
1GB	IFD-25SI001GBCFX[1]	IFD-25SI001GBIFX[1]
2GB	IFD-25SI002GBCFX[1]	IFD-25SI002GBIFX[1]
4GB	IFD-25SI004GBCFX[1]	IFD-25SI004GBIFX[1]
8GB	IFD-25SI008GBCFX[1]	IFD-25SI008GBIFX[1]
16GB	IFD-25SI016GBCFX[1]	IFD-25SI016GBIFX[1]
32GB	IFD-25SI032GBCFX[1]	IFD-25SI032GBIFX[1]
64GB[3]	IFD-25SI064GBCFX[1]	

Notes:
(1) X[1]: Transfer Mode (P: PIO Mode 4 U: UDMA Mode)
(2) 128MB device only for SLC Flash.
(3) 64GB device only for MLC Flash.

8.2 1.8 inch Form Factor

Capacity	Standard Temp.	Wide Temp.
128MB[2]	IFD-18SI128MBCFX[1]	IFD-18SI128MBIFX[1]
256MB	IFD-18SI256MBCFX[1]	IFD-18SI256MBIFX[1]
512MB	IFD-18SI512MBCFX[1]	IFD-18SI512MBIFX[1]
1GB	IFD-18SI001GBCFX[1]	IFD-18SI001GBIFX[1]
2GB	IFD-18SI002GBCFX[1]	IFD-18SI002GBIFX[1]
4GB	IFD-18SI004GBCFX[1]	IFD-18SI004GBIFX[1]
8GB	IFD-18SI008GBCFX[1]	IFD-18SI008GBIFX[1]
16GB	IFD-18SI016GBCFX[1]	IFD-18SI016GBIFX[1]
32GB	IFD-18SI032GBCFX[1]	IFD-18SI032GBIFX[1]
64GB[3]	IFD-18SI064GBCFX[1]	

Notes:
(1) X[1]: Transfer Mode (P: PIO Mode 4 U: UDMA Mode)
(2) 128MB device only for SLC Flash.
(3) 64GB device only for MLC Flash.

8.3 Product Number decoder

$X_1X_2X_3$-$X_4X_5X_6X_7X_8X_9X_{10}X_{11}X_{12}X_{13}X_{14}X_{15}$

$X_1X_2X_3$: Product Name
IFD: IDE Flash Disk

X_4X_5: Form Factor
25: 2.5 inch form factor
18: 1.8 inch form factor

X_6X_7: Product Type
SI: **SMI-SM2231**

$X_8X_9X_{10}X_{11}X_{12}$: Product Capacity
128MB: 128M Byte
256MB: 256M Byte
512MB: 512M Byte
001GB: 1G Byte
002GB: 2G Byte
004GB: 4G Byte
008GB: 8G Byte
016GB: 16G Byte
032GB: 32G Byte
064GB: 64G Byte

X_{13}: Operation Temperature
C: Standard Temperature(0~+70℃)
I: Wide Temperature(-40℃~+85℃)

X_{14}: Disk Mode
F: Fixed Disk Mode
R: Removable Disk Mode

X_{15}: Transfer Mode
P: PIO Mode 4
U: UDMA Mode4